CLAIMS

art A3 1. A circuit, comprising:

a read charge control circuit activated by a read signal and an address; and

a write charge control circuit activated by a write signal and the same or a different address, the read charge control circuit and the write charge control circuit both coupled to common data IO lines.

2. A circuit according to claim 1 wherein the read charge control circuit is a sense amplifier.

3. A circuit according to claim 1 wherein the write charge control circuit transfers charge between the data IO lines and bit lines.

4. A circuit according to claim 1 wherein the write charge control circuit includes only two write controlled gates, a first one of the write controlled gates controlling charge of a bit line and a second one of the write controlled gates controlling charge of a complementary bit line.

5. A circuit according to claim 4 wherein the first and second write controlled gates are both controlled by a write column select line signal.

6. A circuit according to claim 4 wherein the first write controlled gate is coupled directly between the bit line and a data IO line and the second write controlled gate is coupled directly between the complementary bit line and a complementary data IO line.

7. A circuit according to claim 1 wherein the read charge control circuit includes a first read controlled gate controlling charge from a bit line to a complementary data IO line and a second read controlled gate controlling charge from a complementary bit line to a data IO line.

8. A circuit according to claim 7 wherein the first and second read controlled gates are both controlled by a read column select line signal.

9. A circuit according to claim 7 wherein the first read controlled gate is coupled directly between the bit line and the complementary data IO line and the second read controlled gate is coupled directly between the complementary bit line and the data IO line.

10. A circuit according to claim 1 including a data output sense amplifier coupled between a data output buffer and the data IO lines.

11. A circuit according to claim 10 including load transistors shared between the read charge control circuit and the data output sense amplifier.

12. A circuit according to claim 1 wherein the read charge control circuit includes:

a first transistor having a first terminal coupled to a bit line, a second terminal coupled to a complementary data IO line and a third terminal;

a second transistor having a first terminal coupled to a complementary bit line, a second terminal coupled to a data IO line and a third terminal; and

a third transistor having a first terminal coupled to a column select line, a second terminal coupled to the third terminal of the first and second transistor and a third terminal coupled to a first reference voltage.

13. A circuit according to claim 12 wherein the write charge control circuit includes:

a first transistor having a first terminal coupled to a write column select line, a second terminal coupled to the complementary bit line and a third terminal coupled to the complementary data IO line; and

a second transistor having a first terminal coupled to the write column select line, a second terminal coupled to the data IO line and a third terminal coupled to the bit line.

14. A circuit according to claim 13 including a first load transistor having a first terminal coupled to a second reference voltage, a second terminal coupled to the data IO line and a third terminal coupled to a third reference voltage; and a second load transistor having a first terminal coupled to the second reference voltage, a second terminal coupled to the complementary data IO line and a third terminal coupled to the third reference voltage.

15. A circuit, comprising:

a read charge control circuit activated by a read column select line; and

a write charge control circuit activated by a write column select line, the read charge control circuit and the write charge control circuit both coupled to common data IO lines;

a data output sense amplifier; and

load transistors shared by both the read charge control circuit and the data output sense amplifier.

16. A method for controlling a memory control circuit, comprising:

controlling a read charge control circuit according to a read control signal and an address;

controlling a write charge control circuit according to a write control signal and the same or a different address; and

controlling charging to and charging from the same data IO lines using the read charge control circuit and the write charge control circuit.

17. A method according to claim 16 including using only two gates in the write charge control circuit for controlling charge between bit lines and the data IO lines.

18. A method according to claim 17 including using only three gates in the read charge control circuit to control charge between the bit lines and the data IO lines.

19. A method according to claim 18 including using a read column select line to control the read charge control circuit and using a write column select line to control the write charge control circuit.

20. A method according to claim 16 including using a data output sense amplifier to amplify the data IO lines before outputting data from the data IO lines.

21. A method according to claim 20 including sharing load transistors between the data output sense amplifier and the read charge control circuit.

22. A column select line circuit, comprising:

a write control input;

a read control input;

an address input;

a first output;

a second output; and

a control circuit configurable into a first arrangement where the first output is activated according to the write control input and the address input and the second output is activated according to the read control input and the same or a different address input, the control circuit also configurable into a second arrangement that activates the first output according to the address input and either the read control input or the write control input.

23. A column select line circuit according to claim 22 including conducting layers used for configuring the control circuit into the first and second arrangement.

24. A column select line circuit according to claim 23 wherein the conducting layers comprise metal lines or poly-silicon lines.

25. A column select line circuit according to claim 22 including fuses for configuring the control circuit into the first and second arrangement.

26. A column select line circuit according to claim 22 including a memory programmable mode signal used for configuring the control circuit into the first and second arrangement.

27. A column select line circuit according to claim 26 wherein the memory programmable mode signal is generated by a combination of external signals and addresses.

28. A column select line circuit according to claim 26 including path gates controlled by the memory programmable mode signal for enabling or disabling the write control input and the read control input.

29. A column select line circuit according to claim 22 wherein the first output is coupled to a write control circuit and the second output is coupled to a read control circuit in the first arrangement and the first output is coupled to both the write control circuit and the read control circuit in the second arrangement.

30. A method for configuring a column select line circuit, comprising:

configuring the column select line circuit into a first arrangement where a first output is activated according to a read control signal and an address and a second output is activated according to a write control signal and the same or a different address; and

configuring the same column select line circuit into a second arrangement where the first output is activated according to the same or the different address and either the read control signal or the write control signal.

31. A method according to claim 30 including using conducting layers to configure the column select line circuit into the first and second arrangement.

32. A method according to claim 30 including using fuses to configure the column select circuit into the first and second arrangement.

33. A method according to claim 30 including using memory programmable mode signals to configure the column select circuit into the first and second arrangement.

Added A4/

ADD B37